Abstract of the Disclosure:

A semiconductor memory is fabricated with a vertical transistor situated in an upper section of a trench above a trench capacitor. First, an auxiliary insulation layer is applied to the conductive material of an inner electrode or to a connecting material of the trench capacitor. The connecting material is situated on the inner electrode, so that, during an epitaxial deposition, semiconductor material grows only on the uncovered sidewalls in the upper section of the trench. A nitride layer, is deposited conformally and the residual cavity between the inner electrode and the epitaxial semiconductor layer is filled with a doped further conductive material. The nitride layer isolates the epitaxial semiconductor layer from the further conductive material, so that no crystal lattice defects can propagate from there into the epitaxial semiconductor layer. Dopants are outdiffused from the further conductive material into the epitaxial semiconductor layer to form a doping region.

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